ResearchInChina
www.researchinchina.com

ADAS/AD Chip Industry Research Report, 2022

Mar.2022

Abstract

Autonomous driving chip research: In addition to computing power, core IP, software stacks, AI training platforms, etc. are becoming more and more important

L2.5 and L2.9 have achieved mass production for vehicles running on the road, and mass production of L3 and L4 in limited scenarios has become a goal for OEMs in the next stage. In March 2022, the U.S. National Highway Traffic Safety Administration (NHTSA) issued final rules eliminating the need for automated vehicle manufacturers to equip fully autonomous vehicles with manual driving controls to meet crash standards. The United States is expected to introduce more important policies for autonomous driving in the future to guide L3/L4 autonomous driving on the road.

In this context, ADAS/autonomous driving chips have seen a wave of upgrades, and many chip makers have launched or planned to unveil high computing power chips. In January 2022, Mobileye introduced the EyeQ? Ultra?, the company's most advanced, highest performing system-on-chip (SoC) purpose-built for autonomous driving. As unveiled during CES 2022, EyeQ Ultra maximizes both effectiveness and efficiency at only 176 TOPS, with 5 nanometer process technology. Although it looks less potent than chips from rivals Qualcomm and NVIDIA, the cost-effective and high-energy-efficiency EyeQ? Ultra? may still be favored by OEMs.

Mobileye's Autonomous Driving SoC Product Line

Mobileye's Autonomous Driving SoC Product Line

Products	Models	Mass Production Time	Process	CPU Cores	GPU Cores	NPU Computing Power	Typical Power Consumption	Application Scenarios
Mobileye SoC	EyeQ® Ultra™	2025	5nm	12 RISC-V CPU cores	ARM GPU	176TOPS	<100W	L4/L5
	EyeQ6H	2024	7nm	8 cores, 32 threads, MIPS architecture	ARM MALI GPU/Imagination GPU	34TOPS	-	L2/L3
	EyeQ6L	2023	7nm	2 cores, 8 threads, MIPS architecture	ARM MALI GPUs	5TOPS	3W	L2
	EyeQ 5	2021	7nm	8*MIPS	-	24TOPS	10W	L2/L3
	EyeQ 4	2018	28nm	4*MIP Si-Class 1*MIP Sm-Class	6*VMP	2.5TOPS	6W	L2
	EyeQ 3	2014	40nm	4*MIPS	4*VMP	0.256TOPS	2.W	L1/L2

Source: ResearchInChina

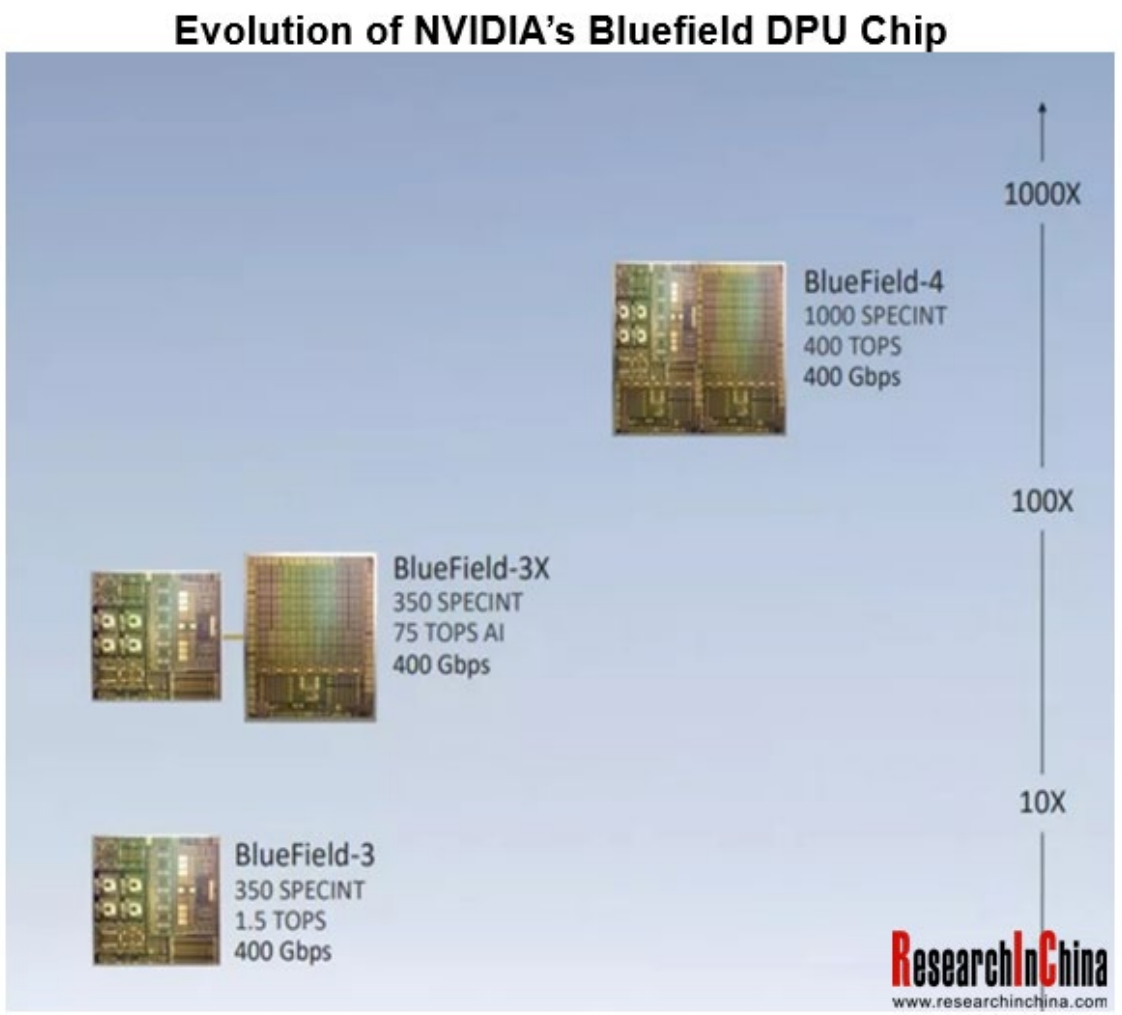
In addition to computing power, self-developed core IP is the focus of competition for major SoC vendors

SoC chips, which are mostly involved with heterogeneous design, include different computing units such as GPU, CPU, acceleration core, NPU, DPU, ISP, etc. Generally speaking, computing power cannot be simply evaluated from the chip alone. Chip bandwidth, peripherals, memory, as well as energy efficiency ratio and cost should be also taken into account. At the same time, the development tool chain of SoC chips is very important. Only by forming a developer ecosystem can a company build long-term sustainable competitiveness.

In chip design, the configuration of heterogeneous IP is crucial, and autonomous driving SoC chip vendors are constantly strengthening the research and development of core IP to maintain their decisive competitive edges. For example, NVIDIA upgraded its existing GPU-based product line to a three-chip (GPU+CPU+DPU) strategy:

- **GPU:** NVIDIA enjoys superiority in GPU and image processing derived from GPU;
- **DPU:** NVIDIA announced the completion of its acquisition of Mellanox Technologies, Ltd., an Israeli chip company, for a transaction value of $7 billion and launched the BlueField?-3 data processing unit (DPU). DPU is a programmable electronic component with the versatility and programmability of a central processing unit (CPU), dedicated to efficiently handling network data packets, storage requests or analysis requests;
- **In terms of CPU,** NVIDIA intended to acquire the semiconductor IP semiconductor ARM as an extension of its three-chip strategy, but it failed in the end. However, NVIDIA launched the Grace? CPU, an Arm-based processor that will deliver 10x the performance of today's fastest servers on the most complex AI and high-performance computing workloads. NVIDIA's next-generation SOC, Atlan, is based on the ARM-based Grace CPU and Ampere Next GPU.

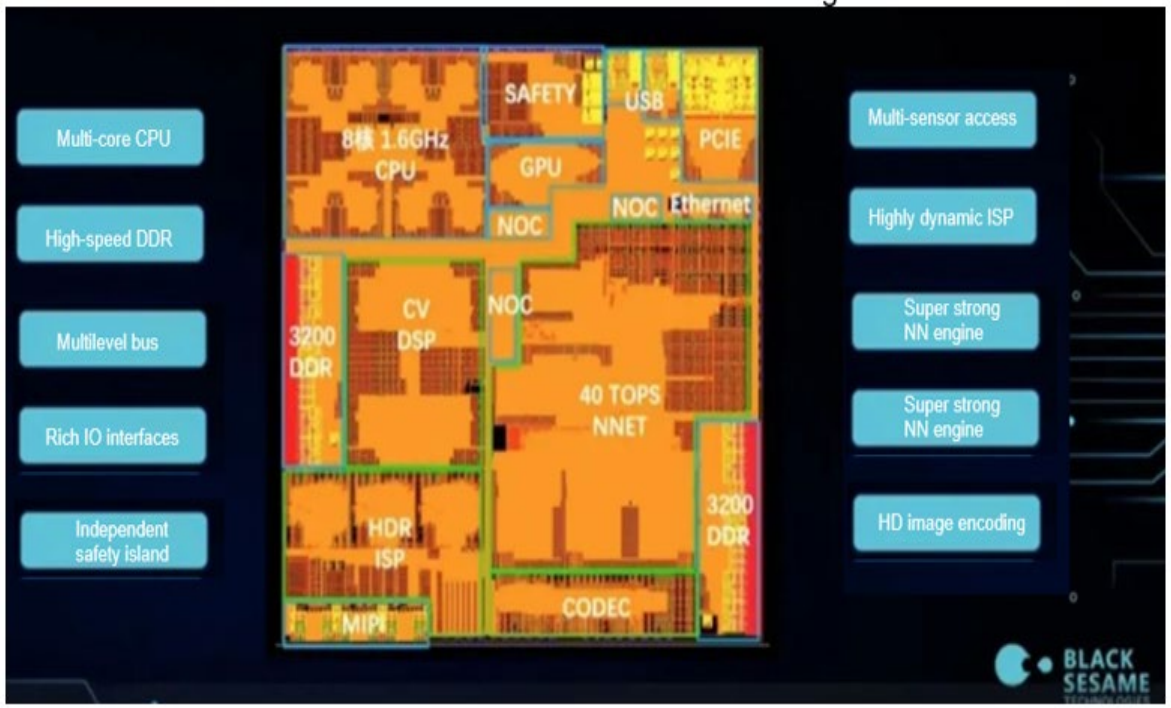
Evolution of NVIDIA's Bluefield DPU Chip



Black Sesame A1000 Autonomous Driving SoC

In terms of domestic vendors, Black Sesame Technologies has launched self-developed NeuralIQ ISP and DynamAI NN engine which is a deep neural network algorithm platform.

Black Sesame A1000 Autonomous Driving SoC



Cross-domain fusion and central computing platform chips will lead the evolution of the automotive EEA

Amid the evolution trend of the automotive EEA: "distributed architecture - domain centralized architecture - cross-domain fusion architecture - central computing platform", Tesla's latest version of Model X has achieved a certain degree of central cross-domain fusion computing. Model X's automotive central computing platform includes two FSD chips, an AMD Ryzen CPU chip and an AMD RDNA2 GPU. The FSD chip and AMD CPU/GPU chip communicate through the PCIe interface and are isolated from each other.

Integrating multiple chips such as CPU, GPU, and FSD into one SoC chip through Chiplet technology will further reduce the chip communication delay. Tesla has reportedly partnered with Samsung on a new 5nm chip for autonomous driving and cockpit SoC chip integration.

The industry’s giants like NVIDIA and Qualcomm have all begun to implement cross-domain integration of autonomous driving and cockpits. For example, NVIDIA has launched DRIVE Concierge and DRIVE Chauffeur for smart cockpits and autonomous driving respectively. DRIVE IX can realize the fusion of algorithms in the cockpit. Based on the powerful software stack tools, NVIDIA's next-generation Ampere architecture (Atlan SoC) will conduct the simultaneous control over autonomous driving and intelligent cockpit with a single chip.

In February 2022, Chinese SoC company Horizon Robotics announced that it will cooperate with UAES to preinstall and mass-produce cross-domain integrated automotive computing platforms.

Cross-domain Fusion/Central Computing Layout

Cross-domain Fusion/Central Computing Layout of Autonomous Driving SoC Vendors

SoC vendors	Layout
Qualcomm Snapdragon Ride SoC and the fourth-generation Snapdragon cockpit chip will enable cross-domain fusion computing	According to the plan, Qualcomm has pushed the manufacturing process to the same starting line for the first time on the 4th generation Snapdragon Automotive Digital Cockpit Platform and the Snapdragon Ride Autonomous Driving Platform, and set the entry threshold for the cross-domain architecture of the next-generation smart cars.
NVIDIA DRIVE Concierge and DRIVE Chauffeur target smart cockpits and autonomous driving respectively. DRIVE IX integrates in-cockpit algorithms.	NVIDIA has not only released the Hyperion 8 autonomous driving reference platform, but also officially launched software platform solutions for the production vehicle market, including DRIVE Concierge for AI assistants and DRIVE Chauffeur for autonomous driving. Cross-domain fusion is possible between DRIVE Concierge and DRIVE Chauffeur. In addition to the autonomous driving part, the Orin SoC development platform has been fully involved with the cockpit, namely DRIVE IX, including driver status monitoring, AR HUD, parking visualization, NLP, virtual machines, electronic rearview mirrors, etc. Based on the next-generation Ampere architecture (Atlan SoC), NVIDIA's partners can implement multiple functions, including cockpit intelligence and autonomous driving, by carrying a single platform and chip, thereby saving multi-platform engineering development costs.
TESLA The next-generation 5nm FSD SoC may enable autonomous driving and cockpit chip integration	In the future, the cockpit domain and the autonomous driving domain may run on the same SoC architecture, because they have many similarities. Tesla is reportedly developing a 5nm chipset with Samsung, which may replace the AMD cockpit computing platform in mass production.

Source: ResearchInChina

SoC vendors accelerate the layout of autonomous driving AI data training

Autonomous driving datasets are critical for training deep learning models and improving algorithm reliability. SoC vendors have launched self-developed AI training chips and supercomputing platforms. Tesla has launched the AI training chip D1 and the "Dojo" supercomputing platform, which will be used for the training of Tesla's autonomous driving neural network.

Besides, training algorithm models are becoming more and more important, including 2D annotation, 3D point cloud annotation, 2D/3D fusion annotation, semantic segmentation, target tracking, etc., such as the NVIDIA Drive Sim autonomous driving simulation platform, the Horizon Robotics "Eddie" data closed loop training platform, etc.

Foreign chip vendors:

- **Tesla** has launched Dojo supercomputing training platform, using Tesla's self-developed 7nm AI training chip D1 and relying on a huge customer base to collect autonomous driving data, so as to achieve model training for deep learning systems. At present, Tesla Autopilot mainly uses 2D images + annotations for training and algorithm iteration. Through the Dojo supercomputing platform, Autopilot can fulfill training through 3D images + time stamps (4D Autopilot system). The 4D Autopilot system will be predictable, and mark the 3D movement trajectory of road objects to enhance the reliability of autonomous driving functions.

- **NVIDIA** has announced NVIDIA Omniverse Replicator, an engine for generating synthetic data with ground truth for training AI networks. NVIDIA also has the most powerful training processor - the NVIDIA A100.

SoC vendors accelerate the layout of autonomous driving AI data training

- The map data of **Mobileye**'s REM has covered the world. In China, Mobileye has solved the compliance problem of map data collection in China through a joint venture with Tsinghua Unigroup. Intel acquired Moovit to enhance the strength and data differentiation of REM, extend the traditional HD map data from the roadside to the user side, start from the perception redundancy of assisted autonomous driving and improve the efficiency of path planning. Intel launched its self-developed flagship AI chip - Ponte Vecchio, which will spread to Mobileye's EyeQ6 (planned for mass production in 2023). In the field of AI and servers, Intel will challenge Nvidia with CO-EMIB technology.

Domestic chip vendors:

- In order to solve the long-tail problem of autonomous driving, **Horizon Robotics** has built a complete data closed-loop platform to iterate algorithms and improve system capabilities. Horizon Robotics has launched the "Eddie" data closed loop training platform.

- **Huawei** has introduced "Octopus" autonomous driving open platform, focusing on the four most critical elements of autonomous driving development - hardware, data, algorithms and HD maps to build a data-centric open platform which prompts closed-loop iterations of autonomous driving. Huawei's Ascend 910 competes with the NVIDIA A100 as the world's top AI training chip. Huawei has also launched the AI training cluster Atlas 900.

Data Training Products of Some Autonomous Driving SoC Chip Vendors

Data Training Products of Some Autonomous Driving SoC Chip Vendors

Autonomous driving SoC vendors	Data training products
NVIDIA	Machine Learning Platform: MAGLEV Autonomous vehicle simulation software: DRIVE Sim AI training chip: A100
TESLA	Tesla Dojo supercomputing training platform Tesla AI supercomputer "ExaPOD" AI training chip D1 and Supercomputing platform "Dojo"
mobileye An Intel Company	REM's map data collection training Moovit's mobility data collection training AI training chip: Ponte Vecchio (Intel)
HUAWEI	"Huawei Octopus" Autonomous Driving Open Platform Architecture Huawei's Ascend 910 AI training chip and Atlas 900 AI training cluster All-Scenario AI Computing Framework: MindSpore
地平线 Horizon Robotics	Horizon Robotics "Eddie" data closed loop training platform.

Comparison of Some Autonomous Driving AI Training Chips

The world's leading autonomous driving AI training chips include: Intel Ponte Vecchio, NVIDIA A100, Tesla D1, Huawei Ascend 910, Google TPU (v1, v2, v3), Cerebras Wafer-Scale Engine, Graphcore IPU, etc.

Comparison of some autonomous driving AI training chips

	Intel Mobileye	Nvidia	Tesla
AI chip	Ponte Vecchio	A100	D1
System architecture	The computing core has at least 8 Xe cores, with the L1 cache of 4MB and TSMC's 5nm process. There are two Xe Link parts, connecting 8 cores respectively, using TSMC's 7nm process, and deserializing up to 90G	Fabricated on TSMC's 7nm N7 manufacturing process, the NVIDIA Ampere architecture-based GA100 GPU that powers A100 includes 54.2 billion transistors with a die size of 826 mm^2. In terms of power consumption, the A100 is rated at 400W while the PCIe is 250W.	It has 50 billion transistors, with the die size of 645 mm^2 and the thermal design power consumption of only 400W
AI computing power	Up to 45TOPS@FP32 at 1.37GHz	A100 supports TF32 operation, with the floating-point performance of 156TFLOPS, the HBM2 video memory and the storage bandwidth of 1.6TB/s	The FP32 single-precision floating-point computing performance can reach 22.6TFlops (22.6 trillion times per second), and the BF16/CFP8 computing performance can hit 362TFlops (362 trillion times per second); All use on-chip SRAM, with the storage bandwidth up to 4TB/s
Packaging process	Intel's exclusive EMIB and Foveros packaging technologies cost far less than TSMC's InFo_SoW, maybe only 1/5 of the cost of Tesla's D1	Flip-Chip MCM Technology	TSMC InFO_SoW (System-on-Wafer), InFO_SoW
Core technology	Intel's Foveros and EMIB	Nvidia's Tensor Core technology yields significant AI acceleration	Tesla's vertical computing system design is very novel, but the core technology of chip manufacturing is still mastered by TSMC

Source: ResearchInChina

Table of Content

Table of Content

Table of Content

Table of Content

Table of Content

Table of Content

Table of Content

Beijing Headquarters
TEL: 13718845418
FAX: 010-82601570
Email: report@researchinchina.com

Website:
www.researchinchina.com

WeChat: zuosiqiche

Chengdu Branch

TEL: 028-68738514
FAX: 028-86930659

zuosiqiche