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# ADAS Domain Controller Key Component Trends Report, 2022

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# CPU

ResearchInChina researched and summarized China's current mainstream high computing power ADAS domain controller products such as Huawei MDC and DJI ADAS domain controller prototype, and technical information.
This paper will briefly analyze the key components of ADAS domain controller, including CPU, MCU, storage, and interface.

## CPU

In terms of CPU selection, to enable their domain controllers to achieve L2+ high-level ADAS functions such as NOP/NGP, all vendors are pursuing large computing power chips, among which Nvidia Xavier and Orin are most used. Both NVIDIA Xavier and Orin incorporate stereo camera hardware acceleration, allowing for direct hardwire output of disparity maps, as well as optical flow acceleration module. The optical flow effect of stereo camera is much better than mono camera. For stereo camera companies, the most core software asset is stereo matching algorithms, most of which are for semi-global matching. Yet it still needs time to explore for better performance.

Depth map is often calculated by CPU. After the depth map, the freespace needs to be calculated, mainly by GPU.

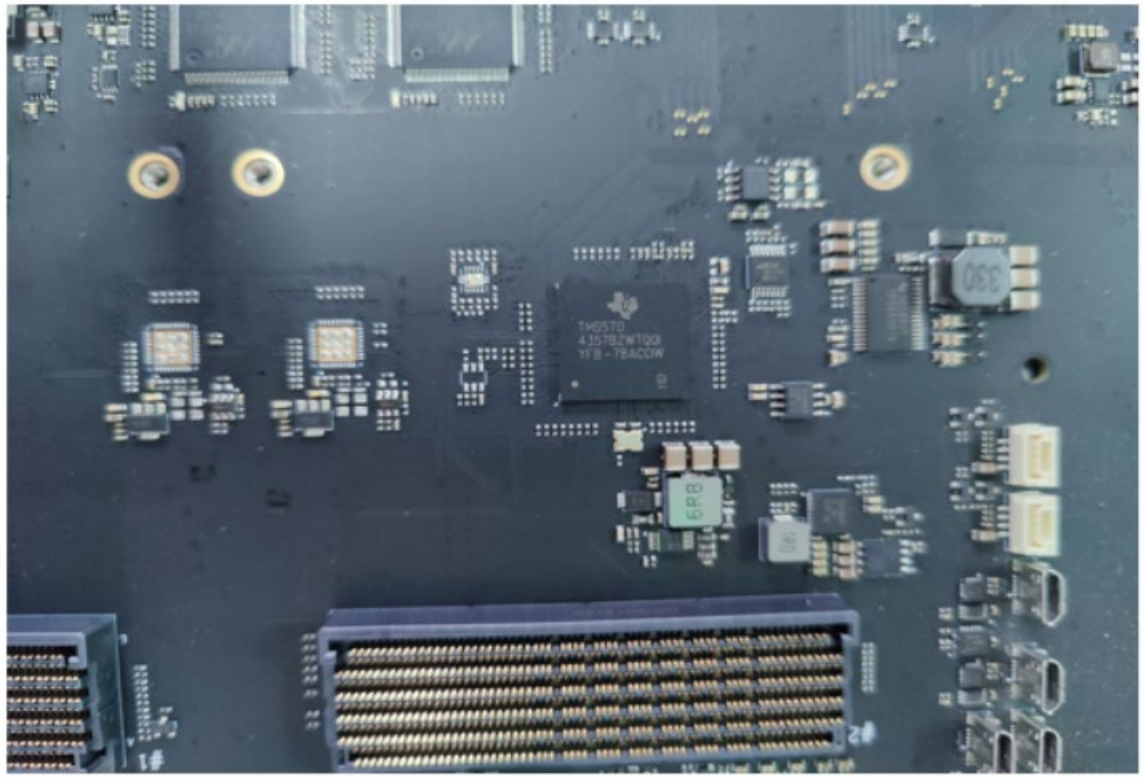
| | Jetson Orin Nano series | | Jetson Orin NX series | | Jetson AGX Orin series | | Jetson AGX Orin Developer Kit |
|---|---|---|---|---|---|---|---|
| | Jetson Orin Nano 4GB | Jetson Orin Nano 8GB | Jetson Orin NX 8GB | Jetson Orin NX 16GB | Jetson AGX Orin 32GB | Jetson AGX Orin 64GB | |
| AI Performance | 20 TOPs | 40 TOPs | 70 TOPS | 100 TOPS | 200 TOPS | 275 TOPS | |
| GPU | 512-core NVIDIA Ampere architecture GPU with 16 Tensor Cores | 1,024-core NVIDIA Ampere architecture GPU with 32 Tensor Cores | 1,024-core NVIDIA Ampere architecture GPU with 32 Tensor Cores | | 1,792-core NVIDIA Ampere architecture GPU with 56 Tensor Cores | 2,048-core NVIDIA Ampere architecture GPU with 64 Tensor Cores | |
| GPU Max Frequency | 625 MHz | | 765 MHz | 918 MHz | 930 MHz | 1.3 GHz | |
| CPU | 6-core Arm® Cortex®-A78AE v8.2 64-bit CPU 1.5MB L2 + 4MB L3 | | 6-core Arm® Cortex®-A78AE v8.2 64-bit CPU 1.5MB L2 + 4MB L3 | 8-core Arm® Cortex®-A78AE v8.2 64-bit CPU 2MB L2 + 4MB L3 | | 12-core Arm® Cortex®-A78AE v8.2 64-bit CPU 3MB L2 + 6MB L3 | |
| CPU Max Frequency | 1.5 GHz | | 2 GHz | | 2.2 GHz | | |
| DL Accelerator | - | | 1x NVDLA v2 | 2x NVDLA v2 | | | |
| DLA Max Frequency | - | | 614 MHz | | 1.4 GHz | 1.6 GHz | |
| Vision Accelerator | - | | 1x PVA v2 | | | | |
| Safety Cluster Engine | - | | - | | - | | |
| Memory | 4GB 64-bit LPDDR5 34 GB/s | 8GB 128-bit LPDDR5 68 GB/s | 8GB 128-bit LPDDR5 102.4GB/s | 16GB 128-bit LPDDR5 102.4GB/s | 32GB 256-bit LPDDR5 204.8GB/s | 64GB 256-bit LPDDR5 204.8GB/s | 32GB 256-bit LPDDR5 204.8GB/s |
| Storage | - (Supports external NVMe) | | | | 64GB eMMC 5.1 | | |

Basic Parameters of Nvidia Orin Chip

# MCU in Domain Controller

Generally, the MCUs for ADAS domain controllers are provided by Infineon or NXP, especially Infineon TC297X/397X series with a high market share. The mainstream MCUs from Renesas, Infineon and NXP all reach the ASIL-D level. For example, the DJI ADAS domain controller engineering prototype MCU uses TI TMS570LC4357, a chip which was launched in 2014 and has not passed ASIL certification but only AEC Q-100 certification.

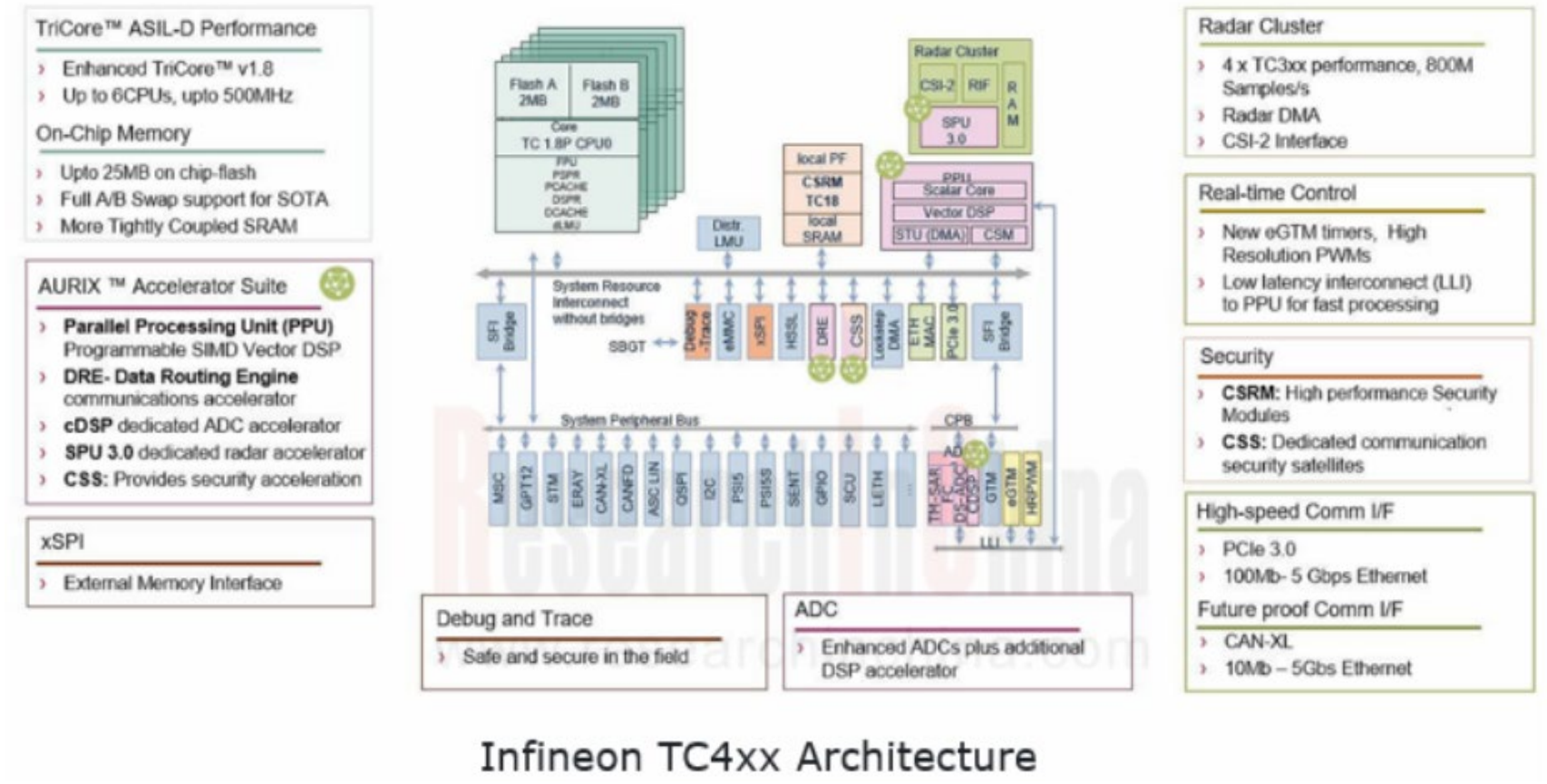
In the second half of 2024, Infineon planned to start mass production of the new AURIX TC4x family of 28 nm microcontrollers (MCUs) for high volume data throughput applications such as advanced driving assistance systems, various domain controllers, new energy and gateway systems.



DJI ADAS Domain Controller Prototype Adopts TI MCU

# MCU in Domain Controller

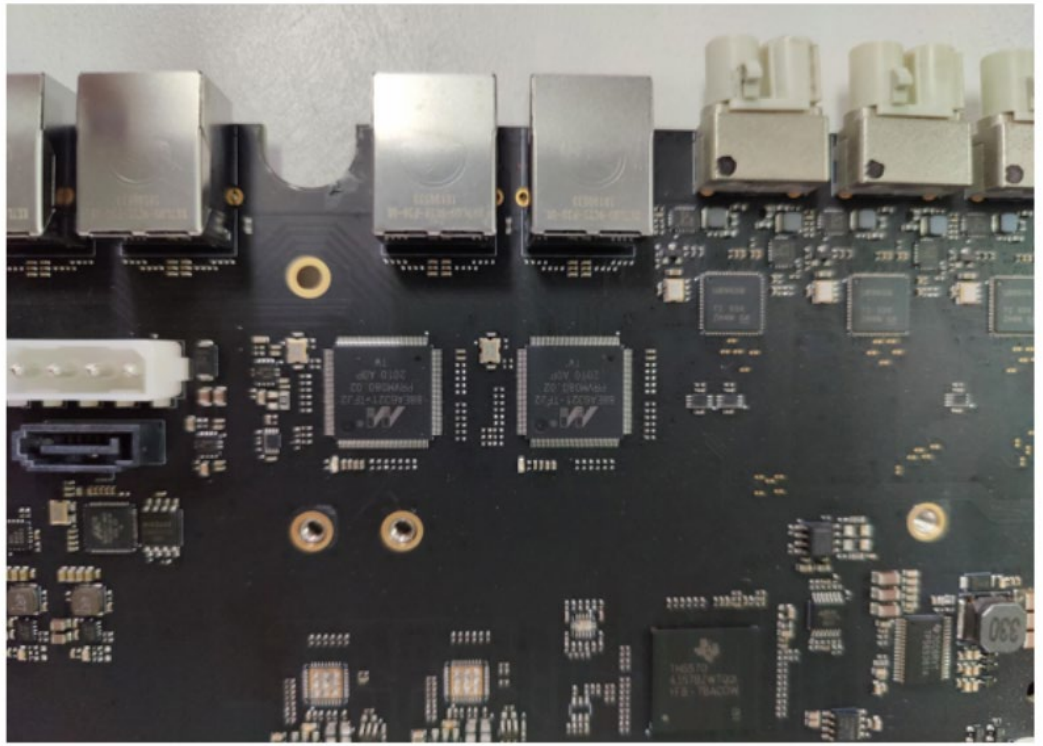
MCU plays a very important role. It is the most important part to ensure the domain controller to achieve ASIL-C/D certification.




Infineon TC4xx Architecture

# Interface

ADAS domain controller needs abundant interfaces (video interface, Ethernet interface, CAN interface, etc.) to connect various sensor devices, including: camera, LiDAR, radar, ultrasonic radar, integrated navigation, IMU, V2X module, etc. Camera interface often uses protocols like GMSL, LVDS and FPDLink. Radar generally adopts CAN/FD communication. LiDAR that needs to upload large amounts of data uses Ethernet interface.



Partial Interfaces and Ethernet Switches of DJI ADAS Domain Controller Prototype

# Interface

Above the DJI ADAS domain controller carrier board MCU are two Ethernet switches, namely, Marvell 88EA6321. On the left is a hard disk SATA interface, using Marvell 88SE9171 chip to convert SATA to PCIe interface. Most development boards don't carry SATA interface, and usually use USB interface. Next to 88SE9171 is a Winbond W25Q64JV NOR Flash with 64Mb capacity, supposed to store a simple hard disk driver.

Marvell's first-generation Automotive Brightlane? Ethernet switch, 88EA6321, is a 7-port Ethernet gigabit capacity switch that is fully compliant with IEEE802.3 automotive standard with Audio/Video bridging capabilities and supports Energy Efficient Ethernet for reduced power consumption. The 7-port Ethernet switch offers 2 integrated IEEE 10/100/1000BASE-T/TX/T ports, 2x RGMII/xMII (2 ports can be configured to be 1GMII) ports, and 1 SGMII / SerDes port. The switch offers remote management capabilities, providing easy access and configuration of the device. It often acts as the bridge between the main processor and the MCU, namely Nvidia Xavier and TI TMS570LC4357.

The 88EA6321 is an early product of Marvell. Marvell's Ethernet switches have now evolved to the third generation. Yet Marvell often cooperates with large manufacturers on advanced products. 88EA6321 targets markets with low security requirements, such as body controllers, Infotainment controllers and gateways, and only supports up to 1G. Although Tesla is also using this chip, new products from conventional automakers such as Volkswagen will not use such a low bandwidth switch. The most advanced design currently available already supports up to 10G, that is, Gigabit Ethernet that generally supports up to 2.5G.

For some LIDARs with high point cloud density, the peak rate may exceed 100M per second. 88EA6321 is not suitable for LIDARs with high point cloud density (it is impossible to use CAN with the maximum available bandwidth only up to 0.5M). At present, the mainstream radars deliver CAN or CAN-FD interface. A very few 4D radars offer optional Ethernet output, and generally the default is CAN-FD.

# Storage

Same as consumer electronics, vehicles have started mass adoption of LPDDR DRAM, UFS, eMMC and other high-speed memory devices to meet the needs of the system and software-level algorithm of ADAS domain controllers for data transmission and storage. At present, the mainstream domain controller storage portfolio mainly applies the form of "LPDDR+UFS", which is consistent with the storage portfolio for smartphones.


Micron Automotive-grade LPDDR5

# Storage

Micron leads the industry in terms of domain controller storage. In June 2021, Micron introduced the first automotive-qualified portfolio of UFS 3.1 memory devices, offering higher cost/density benefits. UFS 3.1 devices enable two times faster read performance and a 50% improvement in sustained write performance than last-generation UFS 2.1 devices. Micron UFS 3.1 meets the needs of growing sensor and camera data for real-time local storage in L3+ ADAS and black box applications. The ADAS domain controller of Li Auto L9 is equipped with Micron's automotive-grade LPDDR5 DRAM memory and UFS 3.1 memory chips based on 3D TLC NAND technology. To date, Micron LPDDR5 is the only ASIL D-certified memory product in the industry.

The higher intelligent driving assistance level, and the gradual application of highway/urban NGP, automated valet parking (AVP) and other functions will pose higher automotive DRAM capacity, bandwidth and product requirements.

***Capacity:*** according to Micron's data, the DRAM capacity required by a single L1/2 vehicle is about 8GB, while that for L3 and L5 vehicles is increased to 16GB and 74GB respectively.

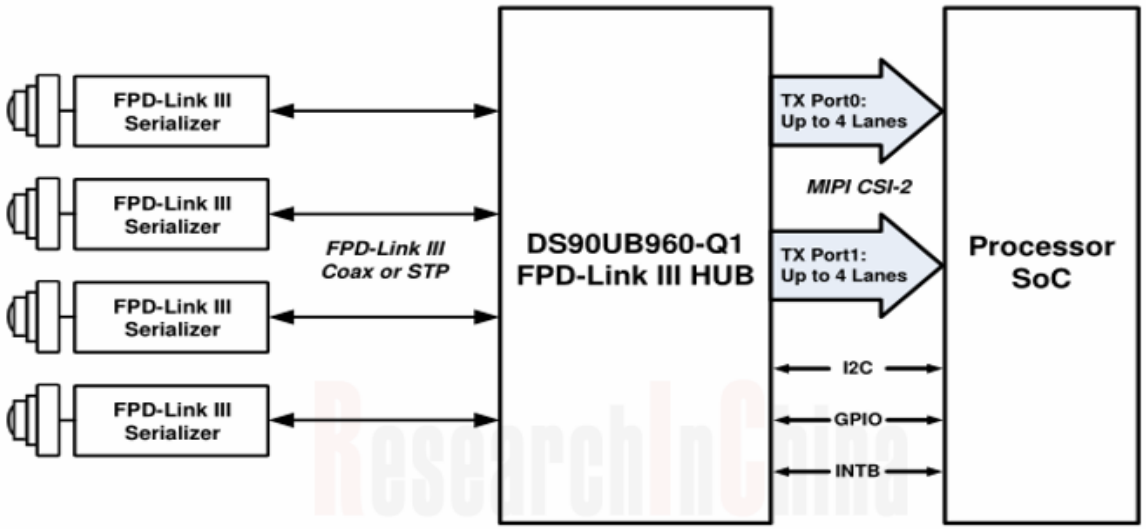
***Bandwidth:*** the DRAM bandwidth for L2 is generally 25-50GB/s; the bandwidth for L3 can reach 200GB/s; and the bandwidth for L4+ will be increased to 1TB/s.

***Product:*** the L2 mainly adopts the basic DDR2/DDR3. At this stage, as L2 starts upgrade to L3, DRAM will also be gradually switched to DDR4 / LPDDR4/LPDDR5/GDDR5.

As for UFS, it is specifically defined by JEDEC as a high-performance memory replacement for e-MMC. It has become the premiere solution for smartphones, continuing to migrate into automotive and other applications. UFS will ultimately surpass e-MMC as the primary storage solution for automotive applications.

# Deserializer

A typical deserializer model is TI DS90UB960. The surround view of the 360° panoramic fisheye camera is usually enabled by Infotainment. The effective distance of the surround view is generally within 10 meters. It is unlikely to be for long distance application in ADAS, and often only for parking. The ADAS domain controller has no requirement for 360° surround view. Besides, one DS90UB960 is enough to correspond to four 360° surround view image sensors.




DS90UB960 Typical Application

The above diagram shows typical applications of TI DS90UB960, that is, receiving YUV444 data from four 2-Megapixel imagers at 30Hz frame rates or YUV420 data from four 2-Megapixel imagers at 60Hz frame rates, more probably the latter. DS90UB954 is a simplified version of DS90UB960, with lanes reduced from 4 to 2. It is generally paired with DS90UB953. It is supposed that Tesla's in-car driver status monitoring uses this chip. For the LVDS output of cameras is not suitable for long-distance transmission, generally cameras should be equipped with a deserializer chip to convert parallel data for serial coaxial or STP transmission, so that the transmission distance can be far and the electromagnetic interference (EMI) is easier to meet automotive regulations.

Here it needs to explain the data formats of cameras, generally RAW RGB and YUV. There are three levels of YUV: YUV444, YUV422 and YUV420. The formula for calculating bandwidth for RAW RGB is: Pixel × Frame Rate × Bit × 4. For example, if a camera outputs 2-megapixel images at 30Hz, the bandwidth is 2 megapixels x30x8x4, or 1.92Gbps, which is too wide. YUV444 is Pixel × Frame Rate × Bit × 3, or 1.44Gbps; YUV422 is Pixel × Frame Rate × Bit × 2, or 0.96Gbps; YUV420 is Pixel × Frame Rate × Bit × 1.5, or 0.72Gbps. For ADAS with low requirements for color, YUV420 is enough. YUV422 finds broad application except in vehicles.

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