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Autonomous Driving SoC Research Report, 2023

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Driving-parking integration boosts the industry, and computing in memory (CIM) and chiplet bring technological disruption.

"Autonomous Driving SoC Research Report, 2023" released by ResearchInChina highlights mainstream automakers' autonomous driving SoC and system deployment strategies, and 9 overseas and 10 Chinese autonomous driving SoC vendors, and discusses the following key issues:

* Analysis and outlook for autonomous driving SoC and system deployment strategies of OEMs;
* Application and configuration strategy of autonomous driving SoC in driving-parking integration;
* Application trends of autonomous driving SoC in cockpit-driving integration;
* Recommended "Turnkey" SoC solutions for autonomous driving;
* Autonomous driving SoC product selection and cost analysis;
* Is it feasible for OEMs to independently make chips (autonomous driving SoC)*
* Application of chiplet in autonomous driving SoC;
* Application of computing in memory (CIM) in autonomous driving SoC.

In driving-parking integration market, single-SoC and multi-SoC solutions have their own target customers.

At this stage, Mobileye still rules the roost in the entry level L2 (intelligent front view all-in-one). In the short term, new products like TI TDA4L (5TOPS) pose a challenge to Mobileye in L2. For L2+ driving and driving-parking integration, most automakers currently adopt multi-SoC solutions. Examples include Tesla's "dual FSD", "triple Horizon J3" on Roewe RX5, "Horizon J3 + TDA4"on Boyue L and Lynk & Co 09, and "dual ORIN" on NIO ET7, IM L7 and Xpeng G9/P7i among others.

According to the production deployment plans of OEMs and Tier 1 suppliers, for lightweight (cost-effective) driving-parking integration, the fusion of driving and parking domains complicates the embedded system design, and poses higher requirements for algorithm model, chip computing power calling (time division multiplexing), computational efficiency of SoC, and costs of SoC and domain control materials.

Some Lightweight Single-SoC Driving-parking Integrated Solutions

Solution Type	Number of SoCs	SoC Solution Portfolio	Computing Power	Sensor Combination	Key Features
Lightweight (cost-effective) driving-parking integrated solution	Single SoC	Single Black Sesame A1000L	16TOPS	5V5R	A1000L is mainly used for image perception and inference, sensor fusion and planning. A1000L allows for access to front view 8MP cameras or 4-channel surround view cameras via two MIPIs at the same time, without needing time-division multiplexing for real driving-parking integrated solutions.
		Single Black Sesame A1000	58TOPS	10V5R (can be configured with 1 LiDAR)	Support NOA and homezone parking pilot or valet parking functions using one or two-channel front view, four-channel surround view and four-channel side view cameras, and enable access to LiDAR and HD maps combined with a SoC for connectivity.
		Single Journey 3	5TOPS	5V5R or 6V5R	Oriented to L2 ADAS, enable a variety of ADAS active safety, comfort and driving assistance functions, and also enable advanced functions such as lane-level navigation, lever shift for lane change, automated parking assist, and remote parking.
		Based on single TDA4VM or TDA4VM Eco	8TOPS	5V5R or 6V5R	Based on single TDA4VM-Q1 or TDA4VM-Q1 Eco, enable a single TDA4-based driving-parking integrated solution with AI compute not higher than 8TOPS. This solution uses time-division multiplexing for driving and parking integration. The "time-division multiplexing" means that it is hard for chips with relatively limited computing power to realize the simultaneous call of the front view cameras and surround view cameras.
		Single TDA4VH or TDA4VM-Q1 Plus	24~32TOPS	10V5R	Based on single TDA4VH or TDA4VM-Q1 Plus, enable a single TDA4-based driving-parking integrated solution with AI compute of 24~32TOPS. The higher computing power allows for access to more cameras.

Source: ResearchInChina

Cost-effective single-SoC solutions, cost-effective multi-SoC solutions and high-end single SoC solutions

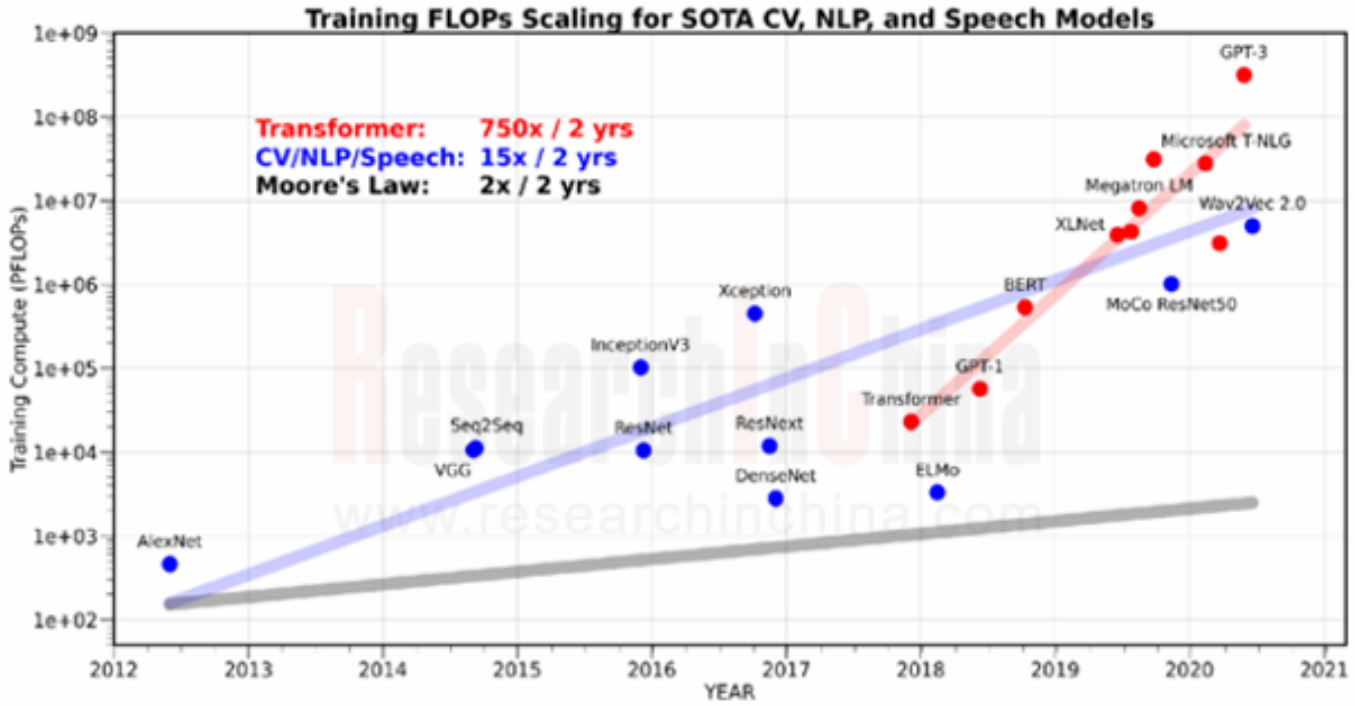
Cost-effective single-SoC solutions: for passenger cars valued at RMB100,000-200,000, the mass production and deployment of the solutions will peak in 2023. The single-SoC driving-parking integrated solutions generally use Horizon J3/J5, TI TDA4VM/TDA4VH/TDA4VM-Q1 Plus, and Black Sesame A1000/A1000L chips. With cost advantages, they can further lower the BOM cost (bill of materials) of entire domain controllers. For example, based on single A1000 SoC and supporting the 10V (camera) NOA function, Black Sesame's driving-parking integrated solution can enable the reduction of the BOM cost of domain controllers to less than RMB3,000, and supports 50-100T physical computing power.

Cost-effective multi-SoC solutions: oriented to passenger cars valued at RMB150,000-250,000, overlapping with those carrying single-SoC solutions, the solutions contain dual TDA4, Horizon J2/J3+TDA4, dual Horizon J3, dual EQ5H, dual Horizon J3+NXP S32G, and triple Horizon J3. Multi-SoC solutions remain superior in safety redundancy and reserve space for OTA updates.
High-level driving-parking integration needs access to more cameras with higher resolution, as well as 4D radars and LiDAR. The BEV+Transformer neural network model is larger and more complex, and may even need to support local algorithm training, so it requires high enough computing power, CPU compute up to at least 150KDMIPS, and AI compute up to least 100TOPS.
High-level driving-parking integration targets high-end new energy vehicles priced at not lower than RMB250,000, with low price sensitivity but higher requirements for power consumption and efficiency of AI chips. In particular, high-compute chips have an impact on the endurance range of new energy vehicles, so that chip vendors have to introduce ever more advanced processes and more energy-efficient chip products.

High-end single SoC solutions: single Horizon J5 and single Black Sesame A1000/A1000 pro solutions gain popularity, and support the application and deployment of 1-2L+11V+5R and leading intelligent driving algorithm models like BEV. In the next stage, single Qualcomm Snapdragon Ride, single Ambarella CV3-AD, and single ORIN chips may also be used by some OEMs as main solutions.
?High-end multi-SoC solutions: dual Nvidia Orin-X and dual FSD are still the mainstream solutions for most of mid- and high-end new energy vehicle models, including the full range of Tesla models, Li Auto L9, Xpeng G9/P7i, IM L7 and Lotus. NIO ET7/ET5 even uses four Orin-X SoCs, two for daily driving computation, and the other two for algorithm training and backup redundancy.

Autonomous driving is facing the contradiction between high computing power and low power consumption, and CIM AI chips may become the ultimate solution.

The popularity of ChatGPT indicates the development directions of autonomous driving: foundation models and high computing power. For large neural network models such as Transformer, the computation will multiply by 750 times every two years on average; for video, natural language processing and speech models, the computation will increase by 15 times every two years on average. It is conceivable that Moore's Law will cease to apply, and the "storage wall" and "power consumption wall" will become the key constraints on the development of AI chips.



Source: CSDN—"Storage Wall", the Achilles' Heel of AI Computing Power

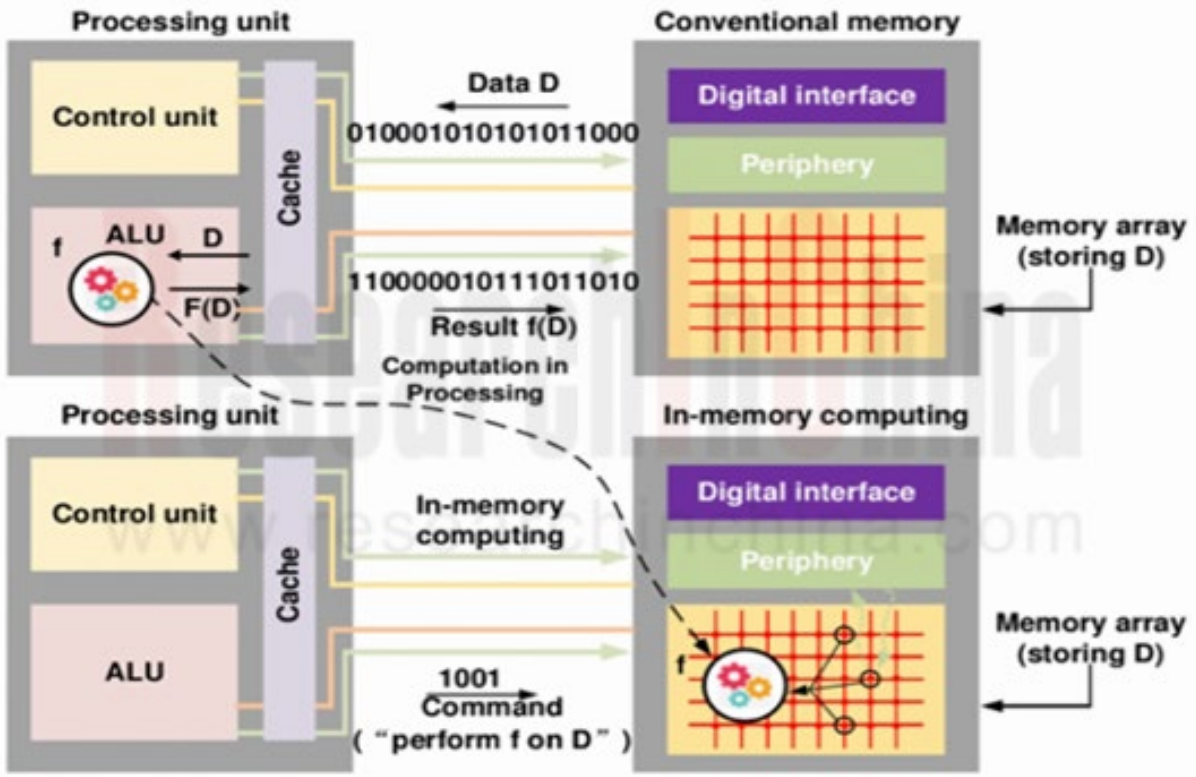
CIM AI chips will be a new technology path option for automakers

At present, most of conventional computing architectures are von Neumann architecture with high flexibility. Yet the problems faced by AI chips are computing power bottleneck and large data transfer, which bring high power consumption.

The computing in memory (CIM) technology is expected to be a solution to the contradiction between high computing power and low power consumption. Computing in memory (CIM) refers to data operation in memory to avoid the "storage wall" and "power consumption wall" caused by data transfer and enable far higher parallelism and energy efficiency of data.

In the automotive field, highly autonomous vehicles will become a running supercomputing center in a sense, with increasing computing power, up to more than 1000TOPS. Cloud computing has sufficient power and can cool down via cooling system, while vehicle edge computing is powered by a battery, facing problems of liquid cooling and cost at the same time.

CIM AI chips will be a new technology path option for automakers.

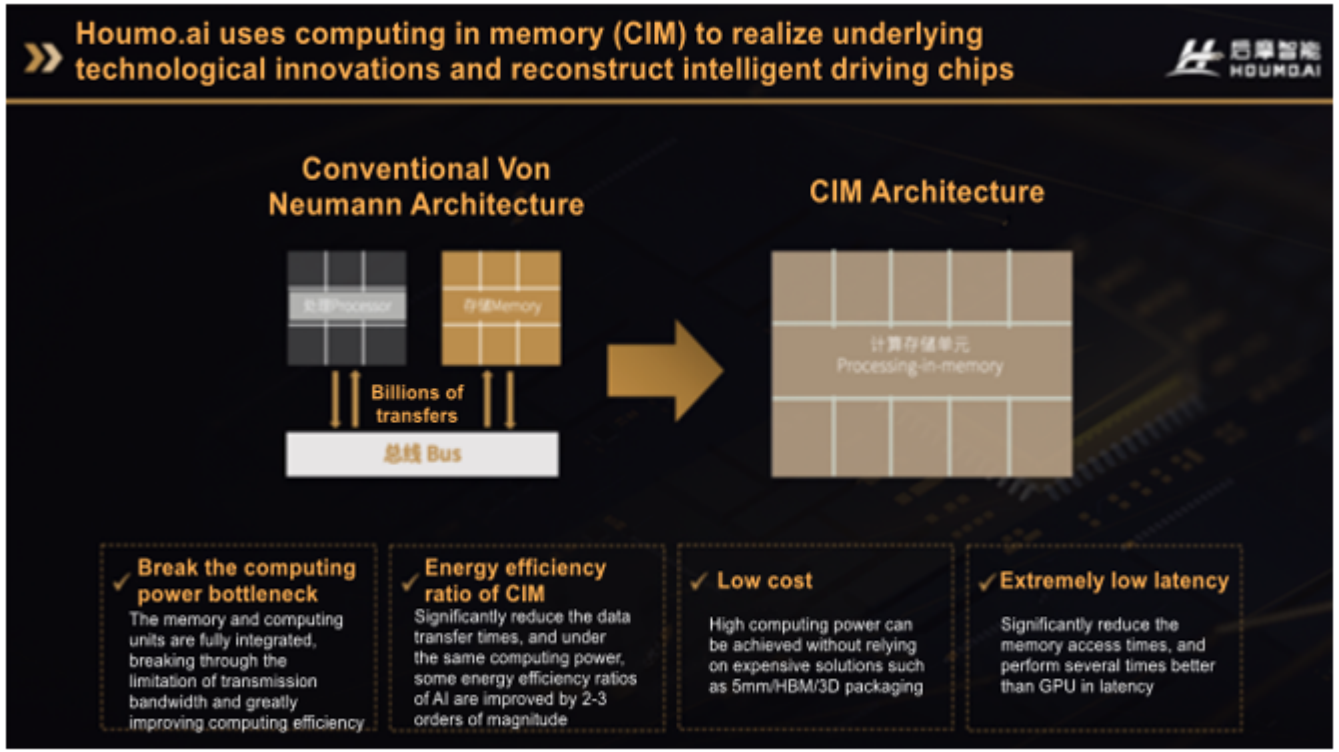


Source: Planet

Houmo.ai is the first autonomous driving CIM AI chip vendor in China

In the field of autonomous driving SoC, Houmo.ai is the first autonomous driving CIM AI chip vendor in China. In 2022, it successfully lightened the industry's first high-compute CIM AI chip on which the intelligent driving algorithm model runs smoothly. This verification sample uses a 22nm process and boasts computing power of 20TOPS, which can be expanded to 200TOPS. Noticeably the energy efficiency ratio of its computing unit is as high as 20TOPS/W. It is known that Houmo.ai will introduce a production-ready intelligent driving CIM chip soon, and we will share its performance in the report.

Differentiated Innovations in Houmo.ai's "Intelligent Driving CIM Chip"



Source: Houmo.ai

Chips will become an investment hotspot for large OEMs.

That OEMs make chips is an extremely controversial issue. In the industry, it is a popular belief that on one hand, OEMs cannot rival specialist IC design companies in development speed, efficiency, and product performance; on the other hand, only when the shipment of a single chip reaches at least one million units can its development cost can be continuously diluted to make it cost-effective.

But in fact, chips have played an absolutely dominant part in intelligent connected new energy vehicles in performance, cost, and supply chain safety. Compared with the typical fuel-powered vehicle that needs 700-800 chips, a new energy vehicle needs 1,500-2,000 units, and a highly autonomous new energy vehicle even needs as many as 3,000 units, some of which are highly valued, high-cost chips that may be in short supply and even out of stock.

It is obvious that large OEMs do not want to be bound by some chip vendor, and they even have already begun to manufacture chips independently. In Geely's case, the automaker has spawned 7nm cockpit SoCs and installed them in vehicles, and has also accomplished IGBT tape-out. The autonomous driving SoC AD1000, jointly developed by ECARX and SiEngine, is expected to be taped out in March 2024 at the earliest.

SoC and Autonomous Driving System Deployment Strategies of Some OEMs

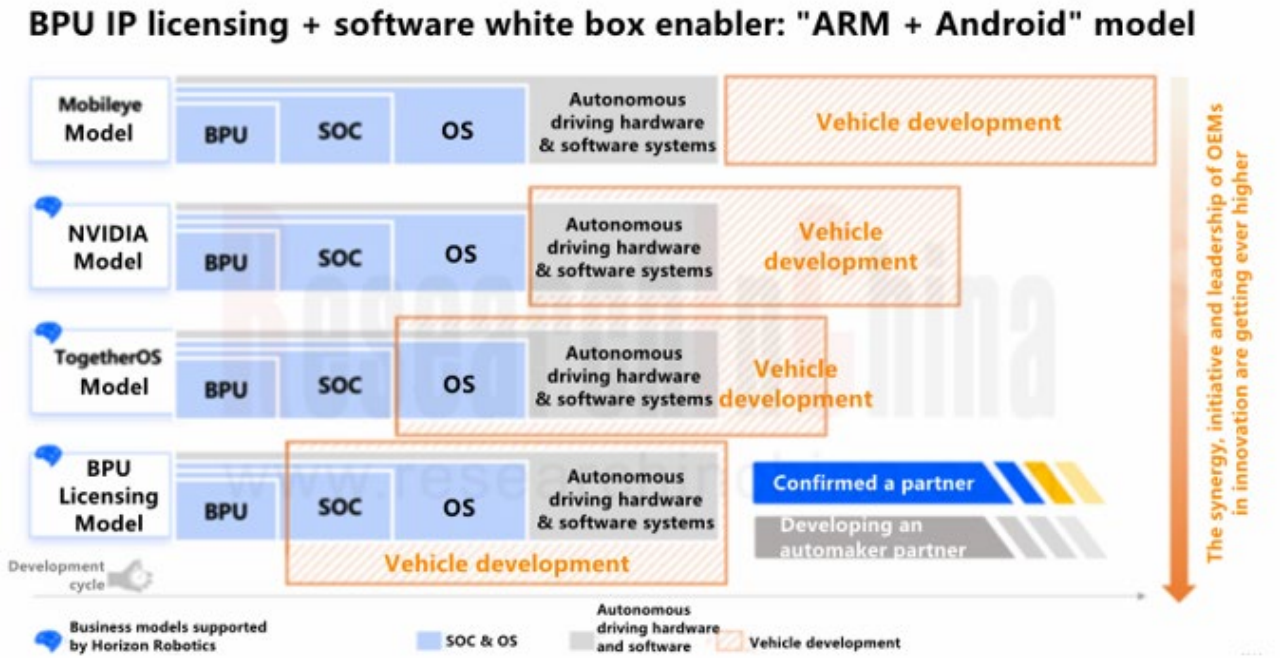
Automaker	Autonomous Driving SoC Solution Portfolio	Total Computing Power for Autonomous Driving	System Integrator	System Solution Configuration	Models with the Solution
Geely	Mobileye EyeQ3/EyeQ4	≤2.5 TOPS	Veoneer	✓ Entry-level L2, intelligent front view all-in-one	Xingyue, Polestar 2, Smart Elf, Volvo XC40, Geometry, etc.
	Mobileye EyeQ5H*2	48 TOPS	iMotion	✓ The sensors include 1 radar, 12 ultrasonic radars and 15 cameras, and the software system is Mobileye SuperVision	ZEEKR 001, ZEEKR 009
	Horizon J3+TI TDA4	13 TOPS	Freetech + Geely	✓ The sensors include 1 front-view camera, 1 rear-view camera, 4 surround-view cameras, 5 radars, 12 long-range ultrasonic radars, and 1 driver monitoring camera.	Boyue L, Lynk & Co 09
	NVIDIA Orin-X*2	508 TOPS	Veoneer	✓ Volvo's next-generation XC90 BEV will use Luminar's third-generation Iris LiDAR, combined with at least 8 cameras, 5 radars, and several ultrasonic sensors.	XC90 BEV (2023 SOP) Smart (2024 SOP)
	NVIDIA Orin-X*2	508 TOPS	Lotus Robotics (co-funded with Momenta)	✓ 4 Hesai AT128 hybrid solid-state LiDARs, 7 8MP cameras, 2 4D imaging radars, 4 radars, 4 2MP surround-view cameras, 12 ultrasonic radars and an interior camera	Lotus Eletre
	Black Sesame A1000+ SiEngine Longying No.1 (cockpit SoC)	58 TOPS	JICA Intelligent	✓ ECARX Super Brain cockpit-driving integrated central computing platform covers various sensor solutions such as 3R1V, 5R6V and 5R10V, can realize NOA function; ✓ Super Brain can reduce 5% vehicle wiring harnesses, 15% R&D cost, and 20% vehicle BOM cost.	Lynk & Co 08 (2023Q3 SOP)
	SiEngine AD1000 (under research)	256 TOPS	JICA Intelligent	✓ ECARX and SiEngine have begun to develop an intelligent driving chip in 2021, which is expected to be taped out in March 2024 at the earliest. It is projected to be called AD1000 initially; ✓ The 7nm intelligent driving SoC integrates ARM's high-end CPU A78 (computing power: 250K DMIPS), DSP and other cores. The AI accelerator can provide maximum INT8 compute of 256TOPS, and has an independent safety island, enabling a good functional safety level, without Infineon TC397.	To be mass-produced and delivered after 2025

Source: ResearchInChina

Chips will strengthen underlying basic capabilities

We predict that ***as with power batteries, chips will become an investment hotspot for large OEMs to strengthen their underlying basic capabilities.*** In 2022, Samsung announced that it will make chips for Waymo, Google's self-driving division; GM Cruise also announced independent development of autonomous driving chips; Volkswagen announced that it will establish a joint venture with Horizon Robotics, a Chinese autonomous driving SoC vendor.

At the China EV100 Forum 2022, Horizon Robotics opened the IP license of BPU (Brain Processing Unit), its high-performance autonomous driving processor architecture on the basis of its business model of "chip + algorithm + tool chain + development platform", in a bid to meet the needs of some automakers with great ability to develop independently, thereby improving their differentiated competitive edges and accelerating their pace of R&D and innovation. As an IP provider that supports automakers to self-develop computing solutions, Horizon Robotics has confirmed a BPU IP licensing model partner and is developing another automaker partner.



Source: Horizon Robotics

Tesla HW 3.0

The technical barriers for chip fabrication are not particularly high. The primary threshold is enough capital and order intake. The chip industry now adopts the block-building model, namely, purchasing IPs to build chips including CPU, GPU, NPU, storage, NoC/bus, ISP and video codec. ***In the future, as chiplet ecosystems and processes get improved, the threshold for independent development of autonomous driving SoCs will be much lower for automakers just need to buy dies (IP chip) directly and then package them, with no need to buy IPs.***

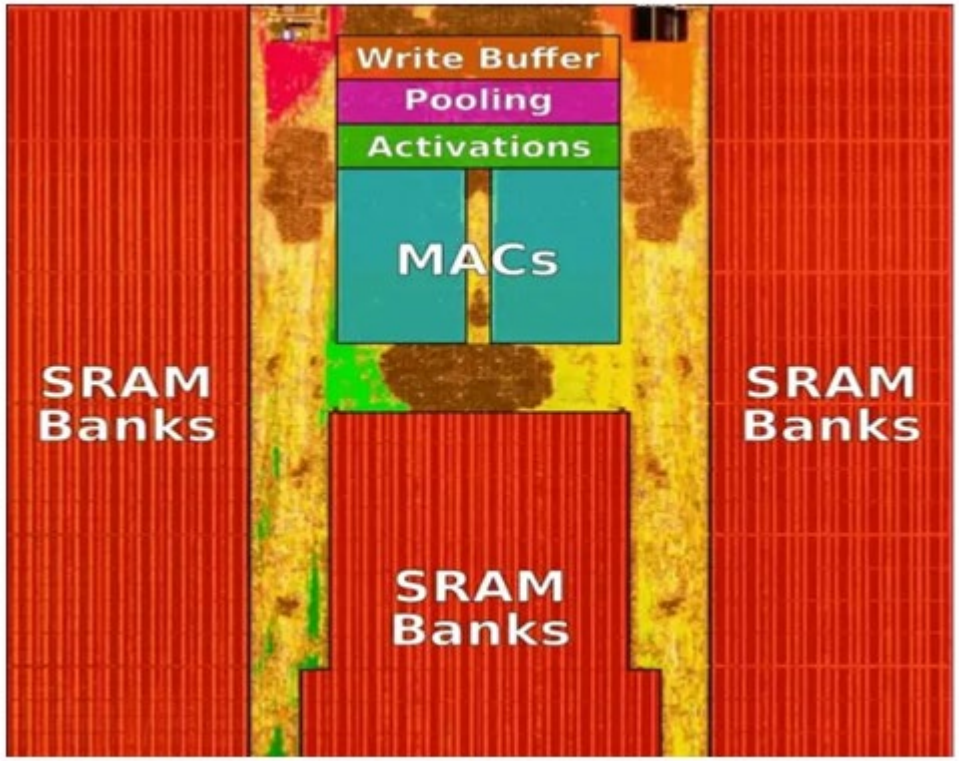
In the case of Tesla HW 3.0, the architecture design is based on Samsung Exynos-IP; the CPU/GPU/ISP design uses ARM's IP; the network-on-chip (NoC) uses Arteris' IP. Tesla only self-develops neural network accelerator (NNA) IP, and the foundry is Samsung.

Tesla deepens its cooperation with Broadcom on HW 4.0 development. To improve AI computing power, the easiest and most effective way is to stack up MAC units and SRAM. For AI operations, the main bottleneck is storage. The disadvantage is that SRAM occupies a large space of chips, and the chip area is however proportional to the cost. Moreover, it is difficult to increase the density and reduce the area of SRAM using advanced processes.

Therefore the area of Tesla's first-generation bare chip FSD HW 3.0 is 260 square millimeters, and the area of the second-generation bare chip FSD HW 4.0 is expected to be up to 300 square millimeters, with the total cost estimated to increase by at least 40-50%. By our estimate, the cost of HW3.0 chips has dropped to USD90-100, and HW 4.0 should cost USD150-200, but even so, Tesla's self-developed chips are far more cost-effective than the bought-in.

In the long run, OEMs with millions of sales are feasible to make chips on their own.

NNA Architecture of Tesla HW 3.0



Source: Tesla

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Contact

Beijing Headquarters
TEL: 010-82601561, 82863481
Mobile: 137 1884 5418
Email: report@researchinchina.com

Website:
www.researchinchina.com

WeChat: zuosiqiche

zuosiqiche

Chengdu Branch

TEL: 028-68738514
FAX: 028-86930659